

CLAIMS

What is claimed is:

- 1 1. A method comprising:
2 reading a performance information associated with a processor;
3 locating a processor performance table that corresponds to the performance
4 information, the performance table including a plurality of performance parameters to
5 control performance of the processor; and
6 updating a performance state (PS) structure using one of the processor performance
7 table and a default table.
- 1 2. The method of claim 1 wherein reading the performance information
2 comprises:
3 reading one of a maximum performance parameter and a minimum performance
4 parameter from a register in the processor.
- 1 3. The method of claim 1 wherein locating the performance table comprises:
2 scanning through a set of performance tables;
3 comparing the performance information with performance indices in the
4 performance tables; and
5 if at least one the performance indices matches with the performance information,
6 copying entries of the processor performance table corresponding to the at least one of the
7 performance indices to a local table, else copying the default table to the local table.
- 1 4. The method of claim 3 wherein updating the PS structure comprises:
2 parsing a source language code containing the PS structure; and
3 replacing entries in the PS structure by the local table.
- 1 5. The method of claim 1 further comprising:
2 updating a checksum for a description table according to an advanced configuration
3 and power management (ACPI) protocol.

1 6. The method of claim 1 wherein reading the performance information
2 comprises:
3 reading a bus ratio parameter and a voltage identifier, the bus ratio parameter
4 corresponding to an operating frequency, the voltage identifier corresponding to an
5 operating power of the processor.

1 7. A method comprising:
2 booting a platform having a processor after a performance state (PS) structure is
3 updated;
4 loading an advanced configuration and power management (ACPI) operating
5 system (OS); and
6 transitioning to a next performance state based on a performance criteria using the
7 PS structure.

1 8. The method of claim 7 further comprises:
2 evaluating the PS structure.

1 9. The method of claim 7 wherein transitioning comprises:
2 reading a current performance information from a status register in a processor;
3 comparing the current performance information with the PS structure to locate a
4 current entry in the PS structure; and
5 obtaining a next entry based on the current entry.

1 10. The method of claim 9 wherein transitioning further comprising:
2 updating a control register associated with performance of the processor using the
3 next entry.

1 11. A computer program product comprises:
2 a machine useable medium having computer program code embedded therein, the
3 computer program product having:
4 computer readable program code to read a performance information
5 associated with a processor;

6 computer readable program code to locate a processor performance table
 7 that corresponds to the performance information, the performance table including a
 8 plurality of performance parameters to control performance of the processor; and
 9 computer readable program code to update a performance state (PS)
 10 structure using one of the processor performance table and a default table.

1 12. The computer program product of claim 11 wherein the computer readable
 2 program code to read the performance information comprises:
 3 computer readable program code to read one of a maximum performance parameter
 4 and a minimum performance parameter from a register in the processor.

1 13. The computer program product of claim 11 wherein the computer readable
 2 program code to locate the performance table comprises:
 3 computer readable program code to scan through a set of performance tables;
 4 computer readable program code to compare the performance information with
 5 performance indices in the performance tables;
 6 computer readable program code to copy entries of the processor performance table
 7 corresponding to at least one of the performance indices to a local table if the at least one
 8 of the performance indices matches with the performance information, and
 9 computer readable program code to copy the default table to the local table if none
 10 of the performance indices matches with the performance information.

1 14. The computer program product of claim 11 wherein the computer readable
 2 program code to update the PS structure comprises:
 3 computer readable program code to parse a source language code containing the PS
 4 structure; and
 5 computer readable program code to replace entries in the PS structure by the local
 6 table.

1 15. The computer program product of claim 11 further comprising:
 2 computer readable program code to update a checksum for a description table
 3 according to an advanced configuration and power management (ACPI) protocol.

1 16. The computer program product of claim 11 wherein the computer readable
2 program code to read the performance information comprises:
3 computer readable program code to read a bus ratio parameter and a voltage
4 identifier, the bus ratio parameter corresponding to an operating frequency, the voltage
5 identifier corresponding to an operating power of the processor.

1 17. A computer program product comprising:
2 a machine useable medium having computer program code embedded therein, the
3 computer program product having:
4 computer readable program code to boot a platform having a processor after
5 a performance state (PS) structure is updated;
6 computer readable program code to load an advanced configuration and
7 power management (ACPI) operating system (OS); and
8 computer readable program code to transition to a next performance state
9 based on a performance criteria using the PS structure.

1 18. The computer program product of claim 17 further comprises:
2 computer readable program code to evaluate the PS structure.

1 19. The computer program product of claim 17 wherein the computer readable
2 program code to transition comprises:
3 computer readable program code to read a current performance information from a
4 status register in a processor;
5 computer readable program code to compare the current performance information
6 with the PS structure to locate a current entry in the PS structure; and
7 computer readable program code to obtain a next entry based on the current entry.

1 20. The computer program product of claim 19 wherein the computer readable
2 program code to transition further comprising:
3 computer readable program code to update a control register associated with
4 performance of the processor using the next entry.

1 21. A system comprising:
2 a processor;
3 a memory coupled to the host to store a system management interrupt (SMI)
4 handler, the SMI handler when executed in response to an SMI, causing the processor to:
5 read a performance information associated with a processor,
6 locate a processor performance table that corresponds to the performance
7 information, the performance table including a plurality of performance parameters
8 to control performance of the processor, and
9 update a performance state (PS) structure using one of the processor
10 performance table and a default table.

1 22. The system of claim 21 wherein the SMI handler causing the processor to
2 read the performance information causes the processor to:
3 read one of a maximum performance parameter and a minimum performance
4 parameter from a register in the processor.

1 23. The system of claim 21 wherein the SMI handler causing the processor to
2 locate the performance table causes the processor to:
3 scan through a set of performance tables;
4 compare the performance information with performance indices in the performance
5 tables; and
6 if at least one of the performance indices matches with the performance
7 information, copy entries of the processor performance table corresponding to the at least
8 one of the performance indices to a local table, else copy the default table to the local table.

1 24. The system of claim 21 wherein the SMI handler causing the processor to
2 update the PS structure causes the processor to:
3 parse a source language code containing the PS structure; and
4 replace entries in the PS structure by the local table.

1 25. The system of claim 21 the SMI handler further causes the processor to:

2 update a checksum for a description table according to an advanced configuration
3 and power management (ACPI) protocol.

1 26. The system of claim 21 wherein the SMI handler causing the processor to
2 read the performance information causes the processor to:
3 read a bus ratio parameter and a voltage identifier, the bus ratio parameter
4 corresponding to an operating frequency, the voltage identifier corresponding to an
5 operating power of the processor.

1 27. A system comprising:
2 a processor in a platform;
3 a system memory coupled to the processor; and
4 a basic input output system (BIOS) memory coupled to the processor, the BIOS
5 memory storing a system management interrupt (SMI) handler, the SMI handler, when
6 executed in response to an SMI, causing the processor to:
7 boot the platform after a performance state (PS) structure is updated, and
8 load an advanced configuration and power management (ACPI) operating
9 system (OS) into the system memory, the ACPI OS, when executed, causing the
10 processor to transition to a next performance state based on a performance criteria
11 using the PS structure.

1 28. The system of claim 27 wherein the ACPI OS, when executed, further
2 causes the processor to:
3 evaluate the PS structure.

1 29. The system of claim 27 wherein the ACPI OS causing the processor to
2 transition causes the processor to:
3 read a current performance information from a status register in the processor;
4 compare the current performance information with the PS structure to locate a
5 current entry in the PS structure; and
6 obtain a next entry based on the current entry.

- 1 30. The system of claim 29 wherein the ACPI OS causing the processor to
- 2 transition further causes the processor to:
- 3 update a control register associated with performance of the processor using the
- 4 next entry.